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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/705,192	11/10/2003	Henry S. Chao	42P17266	5572

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EXAMINER	
HARRISON, MONICA D	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 05/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/705,192	CHAO ET AL.	
	Examiner	Art Unit	
	Monica D. Harrison	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 18-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-17* is/are allowed.

6)☒ Claim(s) *1-10 and 18-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1-25-05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicants amendment filed 9/13/05 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-9, 18-21 and 23-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Osari (6,417,086 B1).

2. Regarding claim 1, Osari discloses a method comprising: forming a logic gate stack in a logic region (Figure 4I, reference 54) on a substrate (Figure 4I, reference 10); forming a flash memory gate stack in a flash region (Figure 4J, references 53-55) on the substrate (Figure 4I, reference 10); depositing a hardmask layer over the logic gate stack and over the flash memory gate stack (Figure 3F, reference 28); patterning the hardmask in the logic region so that areas of hardmask remain where logic gates are desired (Figure 4I, reference 28A); patterning the flash gate stack in the flash region to form flash memory gates (column 11, lines 11-18); and etching the logic gate stack using the remaining hardmask as a mask to form logic gates (column 11, lines 19-39) (Figures 4I, 4J and 8I).

3. Regarding claim 2, Osari discloses wherein the logic region and the flash region are located on a single die (Figure 4H, reference 10).

4. Regarding claim 3, Osari discloses wherein the logic gate stack is comprised of a gate dielectric layer (Figure 3F, reference 22) and a gate electrode layer (Figure 3F, references 26 and 27).

5. Regarding claim 4, Osari discloses wherein the flash memory gate stack is comprised of a gate dielectric layer (Figure 12, reference 122), a floating gate layer (Figure 12, reference 120b), an inter-electrode dielectric layer (Figure 12, reference 126), and a control gate electrode layer (Figure 12, reference 126b; column 1, lines 33-49).

6. Regarding claim 5, Osari discloses removing the hardmask layer column 8, lines 22-52).

7. Regarding claim 6, Osari discloses wherein the hardmask layer consists of an anti-reflective coating (ARC) hardmask layer (column 8, lines 24-33).

8. Regarding claim 7, Osari discloses wherein the ARC hardmask layer is comprised of one or more materials selected from the group consisting of oxide, oxynitride, nitride, and carbon (column 8, lines 24-33).

9. Regarding claim 8, Osari discloses wherein the ARC hardmask layer is sufficiently damaged by the final logic gate stack etch that it may be easily removed (Figure 6D thru Figure 7E).

10. Regarding claim 9, Osari discloses depositing a masking layer over the flash region after patterning the flash gate stack and before etching the logic gate stack to form logic gates (Figure 14E, reference 128).

11. Regarding claim 18, Osari discloses an apparatus comprising: a substrate (Figure 4I, reference 10), the substrate having a logic region (Figure 4I, reference 54) and a flash region

(Figure 4J, references 53-55); a logic gate stack formed on the substrate in the logic region, the logic gate stack having a top surface (Figure 3F, reference 28); regions of antireflective coating (ARC) formed on the top surface of the logic gate stack, the regions of ARC covering the areas of the logic gate stack where logic gates are to be formed (Figure 3F, reference 28); a plurality of flash memory gates formed on the substrate, the flash memory gates having a top surface (Figure 8H); and a layer of resist, wherein the resist covers at least the top surface of the logic gate stack (Figure 14G), the regions of ARC formed on top of the logic gate stack, and the top surface of the flash memory gates (Figure 14G, reference 134).

12. Regarding claim 19, Osari discloses wherein the logic gate stack is comprised of a gate dielectric layer (Figure 3F, reference 22) and a gate electrode layer (Figure 3F, references 26 and 27).

13. Regarding claim 20, Osari discloses wherein the flash memory gate stack is comprised of a gate dielectric layer (Figure 12, reference 122), a floating gate layer (Figure 12, reference 120b), an inter-electrode dielectric layer (Figure 12, reference 126), and a control gate electrode layer (Figure 12, reference 126b; column 1, lines 33-49).

14. Regarding claim 21, Osari discloses wherein the ARC hardmask layer is comprised of one or more materials selected from the group consisting of oxide, oxynitride, nitride, and carbon (column 8, lines 24-33).

15. Regarding claim 23, Osari discloses a method comprising: forming a first stack in a first region (Figure 4I, reference 54) on a substrate (Figure 4I, reference 10) and a second stack in a second region (Figure 4I) on the substrate (Figure 4I, reference 10), wherein the second stack is thicker than the first stack (Figure 4I); depositing a hardmask layer over the first stack

and the second stack (Figure 4I, reference 28A); patterning the first region to remove portions of hardmask in the first region (Figures 3F-3G); patterning the second region to remove portions of the hardmask in the second region and portions of the second stack to form the desired geometries of the second stack (column 11, lines 11-18); and removing portions of the first stack using the remaining portions of hardmask as a mask to form the desired geometries of the first stack Figures (3F-3G).

16. Regarding claim 24, Osari discloses a method comprising: forming a logic gate stack in a logic region (Figure 4I, reference 54) on a substrate (Figure 4I, reference 10); forming a flash memory gate stack in a flash region (Figure 4J, references 53-55) on the substrate (Figure 4I, reference 10); depositing a hardmask layer over the logic gate stack and over the flash memory gate stack (Figure 4I, reference 28); patterning the hardmask in the logic region so that areas of hardmask remain where logic gates are desired (Figures 4I-4J); patterning the flash gate stack in the flash region and etching away the hardmask layer and a portion of the flash memory gate stack in the flash region to form a partial flash memory gate (column 11, lines 11-18); and etching the logic gate stack and the remainder of the flash memory gate stack using the remaining hardmask as a mask to form logic gates and flash memory gates (column 11, lines 19-39; Figures 4I, 4J and 8I).

17. Regarding claim 25, Osari discloses wherein the logic region and the flash region are located on a single die (Figure 4H, reference 10)

18. Regarding claim 26, Osari discloses wherein the hardmask layer comprises an antireflective coating (ARC) hardmask layer (column 8, lines 22-52).

19. Regarding claim 27, Goodwin et al discloses wherein the ARC hardmask layer is comprised of one or more materials selected from the group consisting of oxide, oxynitride, nitride, and carbon (column 8, lines 24-33).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10, 22 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Osari (6,417,086 B1).

20. Osari discloses flash memory gates (Figure 4J, references 53-55) and the logic gate (Figure 4I, reference 54) however, Osari does not disclose the specified length and pitch.

It would have been obvious, at the time the invention was made, for one having ordinary skill in the art, to provide a flash memory gate having a length of less than 150nm and a pitch of less than 400 and a logic gate having a length of less than 150 nm, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the "optimum range" involves only routine skill in the art. ***In re Aller***, 105 USPQ 233 (1955).

Response to Arguments

21. Applicant's arguments with respect to claims 1-10 and 18-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is 571-272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Monica D. Harrison
AU 2813

mdh
May 01, 2006

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